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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/680,664	10/07/2003	Yian-Liang Kuo	24061.43 (TSMC2002-0978)	5418

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EXAMINER	
WILLIAMS, ALEXANDER O	
ART UNIT	**PAPER NUMBER**
2826	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

T14

Office Action Summary	Application No.	Applicant(s)	
	10/680,664	KUO ET AL.	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 August 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,5-11,13-15 and 17-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3, 5-11, 13-15 and 17-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Serial Number: 10/680664 Attorney's Docket #: 24061.43/TSMC2002-0978
Filing Date: 10/7/2003;

Applicant: Kuo et al.

Examiner: Alexander Williams

Applicant's Amendment filed 8/16/07 to the election of species of figure 1 (claims 1 to 3 and 5 to 20), filed 4/12/05, has been acknowledged.

This application contains claim 4 drawn to an invention non-elected without traverse.

Claims 2, 12 and 16 have been cancelled.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation

under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Initially, it is noted that the 35 U.S.C. § 103 rejection based on a plurality of discrete conductors and a plurality of conductive members deals with an issue (i.e., the integration of multiple pieces into one piece or conversely, using multiple pieces in replacing a single piece) that has been previously decided by the courts.

In Howard v. Detroit Stove Works 150 U.S. 164 (1893), the Court held, "it involves no invention to cast in one piece an article which has formerly been cast in two pieces and put together...."

In In re Larson 144 USPQ 347 (CCPA 1965), the term "integral" did not define over a multi-piece structure secured as a single unit. More importantly, the court went further and stated, "we are inclined to agree with the solicitor that the use of a one-piece construction instead of the [multi-piece] structure disclosed in Tuttle et al. would be merely a matter of obvious engineering choice" (bracketed material added). The court cited In re Fridolph for support.

In re Fridolph 135 USPQ 319 (CCPA 1962) deals with submitted affidavits relating to this issue. The underlying issue in In re Fridolph was related to the end result of making a multi-piece structure into a one-piece structure. Generally, favorable patentable weight was accorded if the one-piece structure yielded results not expected from the modification of the two-piece structure into a single piece structure.

Claims 1, 3, 5 to 11, 13 to 15 and 17 to 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shiue et al. (U.S. Patent # 5,700,735).

1. Shiue et al. (figures 1 to 5) specifically figure 3 show an integrated circuit package bond pad, comprising: an insulating layer **44**; an electrode **32** located over the insulating layer and having a plurality of discrete conductors **(first 36 upper portion)** separated by portions of dielectric layer **48**, wherein each of the plurality of discrete conductors has a first surface configured to be bonded to external circuitry and a second surface opposite the first surface; and a plurality of conductive members **(lower portion 36)** located in the insulating layer, wherein ones of the plurality of conductive members physically contact the second surface of corresponding ones of the plurality of discrete conductors of the electrode.

3. The bond pad of claim 1, Shiue et al. show wherein the plurality of conductive members each have a shape selected from the group consisting of: a square cube; a rectangular cube; and a cylinder.

5. The bond pad of claim 1, Shiue et al. show wherein at least two of the ones of the plurality of conductive members have a first size and at least two of the ones of the plurality of conductive members have a second size (both first and second sizes are the same).

6. The bond pad of claim 1, Shiue et al. show wherein the ones of the plurality of conductive members are first ones each having a first shape, wherein second ones of the plurality of conductive members each have a second shape.

7. The bond pad of claim 1, Shiue et al. show wherein each of the plurality of conductive members comprises a material selected from the group consisting of: **metal**;

doped polysilicon; and metal silicide.

8. The bond pad of claim 1, Shiue et al. show wherein at least two of the plurality of conductive members are located in a portion of the insulating layer outside a perimeter of the electrode.

9. The bond pad of claim 1, Shiue et al. show wherein a volumetric ratio of the ones of the plurality of conductive members to the insulating layer ranges between about 1:1 and about 1:5. Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

10. The bond pad of claim 1, Shiue et al. show wherein the first surface of the electrode has a serrated thickness profile.

11. Shiue et al. (figures 1 to 5) specifically figure 3 show a method of manufacturing an integrated circuit package bond pad, comprising: forming an insulating layer **44** over a substrate **40**; forming a plurality of conductive members **(lower portion of 36)** in the insulating layer; and forming an electrode **30** over the insulating layer, the electrode having a plurality of discrete conductors **(upper portion of 36)** separated by portions of a dielectric layer **48**, wherein each of the plurality of discrete conductors has: a first surface configured to be bonded to external circuitry **20,30**; and a second surface opposite the first surface and physically contacting a corresponding one of the plurality of conductive members.

13. The method of claim 11, Shiue et al. show wherein forming the plurality of conductive members includes depositing a material selected from the group consisting of: **metal**; doped polysilicon; and metal

silicide.

14. The method of claim 11, Shiue et al. show wherein the first surface of the electrode has a serrated thickness profile.

15. Shiue et al. (figures 1 to 5) specifically figure 3 show a method of manufacturing an electronic device, comprising: providing a substrate **40** having a first bond pad **30** located thereon; providing an integrated circuit package having a second bond pad **32** located thereon, the second bond pad including: an insulating layer **44**; an electrode **30** located over the insulating layer and having a plurality of discrete conductors **(upper portion of 36)** separated by portions of a dielectric layer **48**, wherein each of the plurality of discrete conductors has a first surface configured to be bonded to the first bond pad and a second surface opposite the first surface; and a plurality of conductive members **(lower portion of 36)** located in the insulating layer, wherein ones of the plurality of conductive members physically contact the second surface of corresponding ones of the plurality of discrete conductors of the electrode; and forming a bond electrically coupling the first and second bond pads.

17. The method of claim 15, Shiue et al. show wherein the plurality of conductive members each have a rectangular cube shape.

18. The method of claim 15, Shiue et al. show wherein a volumetric ratio of the ones of the plurality of conductive members to the insulating layer ranges between about 1:1 and about 1:5. Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575,

1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

19. The method of claim 15, Shiue et al. show wherein the first surface of the electrode has a serrated thickness profile.

20. The method of claim 15, Shiue et al. show wherein forming a bond includes a process selected from the group consisting of: wire bonding; and surface mounting.

Therefore, it would have been obvious to one of ordinary skill in the art to use the plurality of discrete conductors and the plurality of conductor members as "merely a matter of obvious engineering choice" as set forth in the above case law.

Claims 1, 3, 5 to 11, 13 to 15 and 17 to 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Batra et al. (U.S. Patent # 6,909,196 B2).

1. Batra et al. (figures 1 to 4B) specifically figure 4B show an integrated circuit package bond pad, comprising: an insulating layer **ILD2**; an electrode **22** located over the insulating layer and having a plurality of discrete conductors **(upper portion of 24)** separated by portions of dielectric layer **ILD2**, wherein each of the plurality of discrete conductors has a first surface configured to be bonded to external circuitry and a second surface opposite the first surface; and a plurality of conductive members **(lower portion of 24)** located in the insulating layer, wherein ones of the plurality of conductive members contact the second surface of corresponding ones of the plurality of discrete conductors of the electrode.

3. The bond pad of claim 1, Batra et al. show wherein the plurality of conductive members each have a shape selected from the group consisting of: **a square cube**; a rectangular cube; and a cylinder.

5. The bond pad of claim 1, Batra et al. show wherein at least two of the ones of the plurality of conductive members have a first size and at least two of the ones of the plurality of conductive members have a second size (both first and second sizes are the same).

6. The bond pad of claim 1, Batra et al. show wherein the ones of the plurality of conductive members are first ones each having a first shape, wherein second ones of the plurality of conductive members each have a second shape.

7. The bond pad of claim 1, Batra et al. show wherein each of the plurality of conductive members comprises a material selected from the group consisting of: **metal**; doped polysilicon; and metal silicide.

8. The bond pad of claim 1, Batra et al. show wherein at least two of the plurality of conductive members are located in a portion of the insulating layer outside a perimeter of the electrode.

9. The bond pad of claim 1, Batra et al. show wherein a volumetric ratio of the ones of the plurality of conductive members to the insulating layer ranges between about 1:1 and about 1:5. Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

10. The bond pad of claim 1, Batra et al. show wherein the first surface of the electrode has a serrated thickness profile.

11. Batra et al. (figures 1 to 4B) specifically figure 4B show a method of manufacturing an integrated circuit package bond pad, comprising: forming an insulating layer **ILD2** over a substrate **12**; forming a plurality of

conductive members **(lower portions of 24)** in the insulating layer; and forming an electrode **22** over the insulating layer, the electrode having a plurality of discrete conductors **(upper portions of 24)** separated by portions of a dielectric layer **ILD2**, wherein each of the plurality of discrete conductors has: a first surface configured to be bonded to external circuitry; and a second surface opposite the first surface and contacting a corresponding one of the plurality of conductive members.

13. The method of claim 11, Batra et al. show wherein forming the plurality of conductive members includes depositing a material selected from the group consisting of: **metal**; doped polysilicon; and metal silicide.

14. The method of claim 11, Batra et al. show wherein the first surface of the electrode has a serrated thickness profile.

15. Batra et al. (figures 1 to 4B) specifically figure 4B show a method of manufacturing an electronic device, comprising: providing a substrate **12** having a first bond pad **20** located thereon; providing an integrated circuit package having a second bond pad **22** located thereon, the second bond pad including: an insulating layer **ILD2**; an electrode **20** located over the insulating layer and having a plurality of discrete conductors **(upper portion of 24)** separated by portions of a dielectric layer **ILD1** in each of the plurality of discrete conductors has a first surface configured to be bonded to the first bond pad and a second surface opposite the first surface; and a plurality of conductive members **(lower portions of 24)** located in the insulating layer, wherein ones of the plurality of conductive members contact the second surface of corresponding ones of the plurality of discrete

conductors of the electrode; and forming a bond electrically coupling the first and second bond pads.

17. The method of claim 15, Batra et al. show wherein the plurality of conductive members each have a rectangular cube shape.

18. The method of claim 15, Batra et al. show wherein a volumetric ratio of the ones of the plurality of conductive members to the insulating layer ranges between about 1:1 and about 1:5. Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

19. The method of claim 15, Batra et al. show wherein the first surface of the electrode has a serrated thickness profile.

20. The method of claim 15, Batra et al. show wherein forming a bond includes a process selected from the group consisting of: wire bonding; and surface mounting.

Therefore, it would have been obvious to one of ordinary skill in the art to use the plurality of discrete conductors and the plurality of conductor members as "merely a matter of obvious engineering choice" as set forth in the above case law.

Response

Applicant's arguments filed 8/16/07 have been fully considered, but are moot in view of the new grounds of rejections detailed above.

The insertion of Applicant's additional claimed language, for example, "in claim 1, 1, 11 and 15" cause for further search and consideration to make this action final.

Applicant's amendment necessitated the new grounds of rejection. Accordingly, **THIS ACTION IS MADE FINAL**. See M.P.E.P. ∋ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. ∋ 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R. э 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/758,701,700,698,696,781,784,786,774,734,773,779,780, 750,751,173,e23.03,e21.508,e23.144,e23,167,e23.02,e23.152 438/613,617,612,624,626,639,637	6/24/05 12/8/05 1/2/07 6/8/07 8/16/07
Other Documentation: foreign patents and literature in 257/758,701,700,698,696,781,784,786,774,734,773,779,780, 750,751,173,e23.03,e21.508, e23.144,e23.167, e23.02, e23.152 438/613,617,612,624,626,639,637	6/24/05 12/8/05 1/2/07 6/8/07 8/16/07
Electronic data base(s): U.S. Patents EAST	6/24/05 12/8/05 1/2/07 6/8/07

	8/16/07

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571) 272 1236. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
10/24/07